Deep Reactive Ion Etching for Lateral Field Emission Devices

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***Abstract*—This letter describes the design, fabrication and testing of lateral field emission diodes utilizing the deep reactive ion etch (DRIE). Devices were fabricated on silicon-on-insulator (SOI) wafers of varied thickness, by etching the device silicon in the STS DRIE system in a single mask process. After subsequent oxidation sharpening and oxide removal, diodes were tested on a probing station under vacuum. A typical diode exhibited very high currents on the order of $\sim$100 μA at 60 V, and turn-on voltage between 35 V and 40 V. The high electron current is emitted in such a diode by multiple sharp tips vertically spaced by 450 nm along the etched sidewall due to the pulsed nature of the DRIE process.**

I. Introduction

THE research field of vacuum microelectronics strives to combine the best features of highly-advanced solid state fabrication technology and vacuum tube electronics [1], [2]. The goals and potential applications vary from high-temperature and high-radiation amplifiers; RF oscillators and amplifiers and field emitter displays [2]–[5], to a variety of sensors such as ion gauges [6]. To date, the proposed and fabricated field emission devices (FED's) have been largely divided into two groups: vertical and lateral structures. Vertical FED's were frequently fabricated by the use of silicon or Spindt-type metal tips [3], [4]. To our knowledge, the achievable currents per tip with Si as emitting material have been limited to below or the order of 1 μA. Hence, in most proposed applications, large field emitter arrays (FEA's) of up to tens of thousands of tips are required to achieve milliamps of electron current. Significantly higher currents have been achieved by the use of metals with lower work functions [4]. FEA's are commonly characterized by turn-on voltages above 60 V.

Lateral field emission devices (LFED's) [5], [7]–[10] may have many advantages in high-speed and RF applications owing to the simple fabrication and precise control of electrode distances, and have been demonstrated with relatively high current densities, and turn-on voltages as low as 22 V [7]. Lateral Si emitters with currents on the order of tens of microamps per tip have been demonstrated.

The fabrication methodology presented in this work allows for more than an order of magnitude increase in achievable current for each individual device than in the previous work with silicon emitters. With the use of deep reactive ion etch [11] (DRIE,) which cyclically alternates between etch and deposition steps forming scalloped sidewalls, each fabricated lateral device can consist of dozens of tips vertically stacked with submicron distance. The methodology is very simple, and in the case of the presented work, it requires only one mask, one etch and an oxidation step and oxide removal. It also provides for very accurate electrode distance control via photolithography and oxidation self-alignment. Consequently, diodes with turn-on voltages between 35 and 40 V emitting currents up to 400 μA were fabricated in a 2 μm process.

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II. Fabrication and Measurement Setup

Test devices were fabricated in the Berkeley Microfabrication Facility [12] on three different SOI wafers of the following device layer thicknesses: 15 μm, 22 μm, and 30 μm. In each case, the device layer was p-type silicon of 1–10 $\Omega\cdot$ cm resistivity, while the insulating layer was thermally grown wet oxide of 1 μm thickness. It is expected that n-type Si would produce more current due to the lower work function, however, due to their availability at the time of fabrication, p-type SOI wafers were used.

A photograph of a typical diode layout is shown in Fig. 1(a). The layout consists of a device region etch trench—an acute angle cathode and an anode, and a surrounding 8 μm wide isolation trench. The latter is used to isolate the diode from rest of the wafer and to minimize exposed Si area during DRIE, which significantly improves the etch rate, and the etch uniformity. Due to relatively thick device layers, photoresist of 2.6 μm thickness was used. After photolithography with a 10$\times$ stepper and photoresist hardbake, the wafers were etched in the STS DRIE system. The recipe used applies 800 W in the top RF coil for plasma forming and 150 W in the bottom RF platen for reactive ion etching. It switches between etch and deposition steps to achieve high aspect ratio structures [11]—each cycle in our case consists of a 7 s etch followed by a 9 s deposition of passivating teflon. The etch is nearly isotropic, resulting in scalloped sidewalls as illustrated in Fig. 1(b). Average etch rate is around 2.7 μm/min, and the etch is terminated when the SiO_2 layer is reached as shown in Fig. 1(b). With the above recipe, used in all the presented devices, vertical tip density between 2.0 and 2.2 tips/μm was achieved. Namely, for a 15 μm thick SOI device layer, this process produces approximately 30 tips along the etched sidewall.

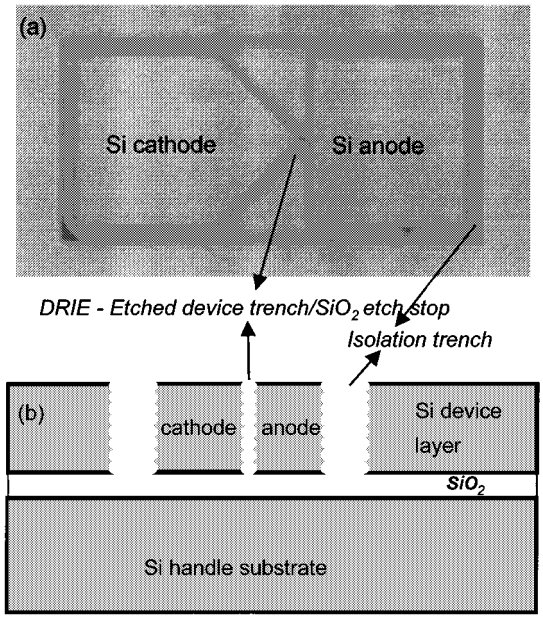

Fig. 1. Fabrication of LFED's by DRIE etching of SOI wafers: (a) microphotograph of the top view of a diode test structure, and (b) schematic cross section of the SOI wafer after DRIE showing exaggerated scalloped sidewalls.

After the DRIE, the wafers were cleaned in a piranha bath to remove the remaining teflon passivation and prepare for oxidation. Fig. 2 shows the two main types of test structures on a wafer at this point in the process. The diode in Fig. 2(a) was designed such that cathode and anode are still in contact until they are separated by silicon removal by oxidation, i.e., self-aligned [7], while the diode in Fig. 2(b) was designed such that the photolithography defines the cathode-anode separation. Most importantly, the so-called scalloped sidewalls after DRIE are visible in the figure, vertically spaced at about 0.45 μm. Subsequently, wafers were oxidized at 900 °C in pyrogenic steam to 5000 A, and in dry oxygen for additional 1000 A of oxide, removing a total of 0.26 μm of Si. The dry oxidation was followed by a 30–min anneal in nitrogen.

Finally, the thermal oxide was removed in buffered oxide etch (BOE 5:1.) The oxide was overetched to slightly undercut the oxide underneath the device layer, up to 1 μm. The final device structure under SEM is shown in Fig. 3. We attempted to measure the radius of a typical tip at up to 300 000× magnification in a FESEM, but the sharpness was beyond the limits of the microscope. It is clear, however, that the radius is less than a few nanometers. This vertical spacing of the tips is a direct function of the etch and passivation time in each DRIE cycle and varies through modifications in the recipe. Our future goal will be to explore such variations, and to eventually significantly increase the number of vertically stacked tips per micron.

Measurements were performed on a probing station under 10^{-5} torr vacuum with a standard semiconductor parametric analyzer, the HP4145. The vacuum was attained by a turbo pump, and was the highest available for such measurements. However, because maximum spacing of any measured cathode-anode pair was within 2 μm, the effect of pumping beyond 10^{-3} could not be seen in short term.

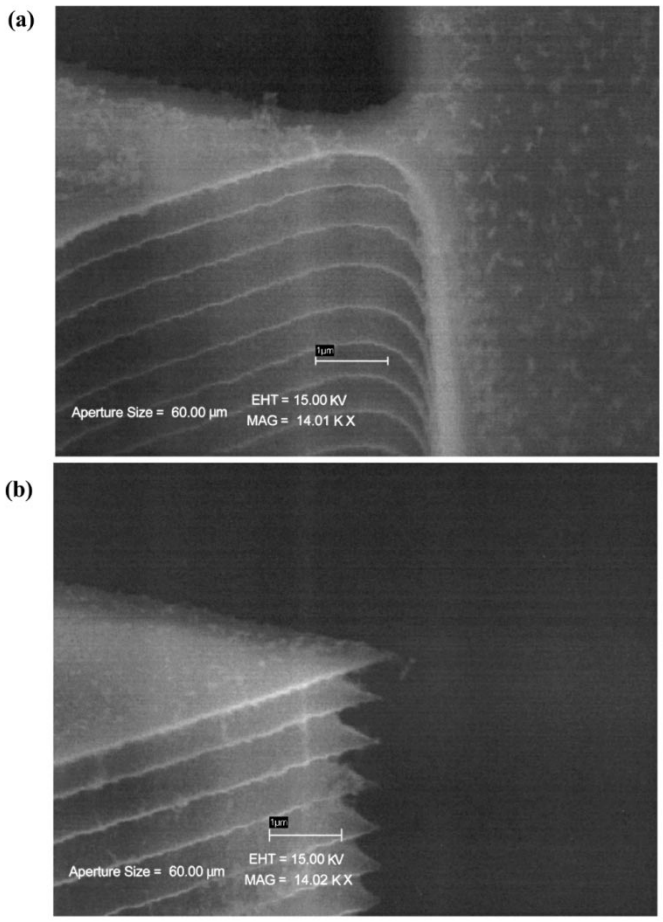

Fig. 2. SEM images of two types of LFED's after DRIE etching, showing the scalloped etch profile due to pulsed etching (a) electrodes in contact for oxidation self-alignment, and (b) electrodes separated by photolithography. Passivation is still seen remaining on the surface.

III. Discussion of the Results

Fig. 4 shows typical measured current-voltage characteristics for the three types of diodes. Devices A, and B, from a 15 μm thick SOI wafer, closely fit the Fowler–Nordheim (FN) emission equation: $I = AV^2 \exp(-B/V)$. The self-aligned diode shows higher current corresponding to extracted parameters $A = 3.58 \cdot 10^{-8}$ and $B = 28.75$. The higher current is most likely due to the closer cathode-anode spacing of approximately 0.8 μm in this case. The extracted FN parameters for the pre-aligned device were $A = 3.21 \cdot 10^{-8}$ and $B = 18.43$. The cathode-anode spacing was 1.2 μm. Approximately 30 tips are vertically stacked in each case.

The device with best performance over the three wafers was a self-aligned diode with 0.8 μm cathode-anode distance, on a 30 μm SOI wafer (resulting in $\sim$60 vertically stacked tips). The *I–V* characteristics, shown in Fig. 4, show 300 μA current at 60 V, and a turn on voltage of approximately 38 V. This device was measured under vacuum and in air, and parameters $A = 2.54 \cdot 10^{-7}$ and $B = 68.61$ were extracted from an FN-fit.

IV. Conclusions

We have reported a novel methodology for fabrication of field emission devices which achieve currents over an order of

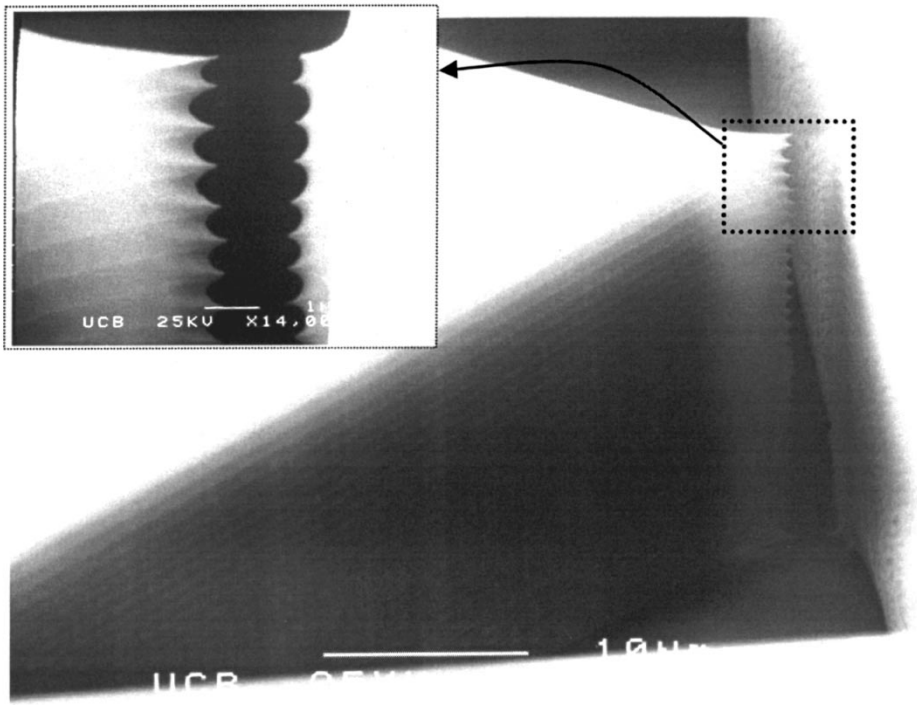

Fig. 3. Scanning electron microscope images of a lateral field emission diode after DRIE etching and oxidation sharpening, showing multiple tips along the vertical edge. Both images were taken at 25 kV, the main image at 2500×, and the inset at 15 000× magnification.

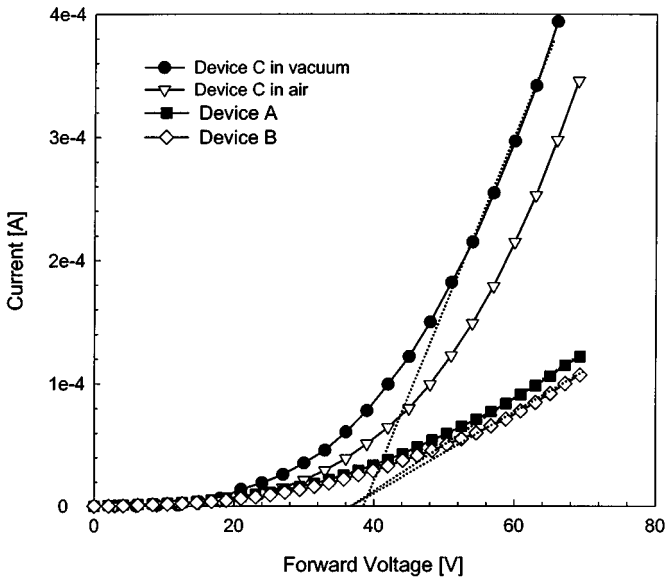

Fig. 4. Measured *I–V* characteristics of three typical devices: Device A is selfaligned anode cathode at 0.8 μm separation, Device B was photolithographically aligned at 1.2 μm separation, and Device C (in vacuum and in air) was selfaligned anode cathode at 0.8 μm separation.

magnitude higher than achievable using previously proposed methods. The characterization confirms that the method of micromachining lateral tips using DRIE holds promise for applications in vacuum microelectronics. The results invite much future effort in thorough characterization and optimization of the process, as well as employing the process to triodes, vacuum sensors, and other applications [13].

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